Performance Analysis Of Three Level Diode Clamped Inverter For Power Quality Issues In Solar PV Grid Connected System

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Abstract: The continuous supply of clean electrical power has become essential to modern civilization. However, the grid and transmission network may not always deliver clean and reliable power. Understanding the variety of power quality problems in the received supply and the nature of the loads is the first approach to the power quality solution. In this paper performance of the diode clamped three-level inverter (DC-TLI) using simulation and hardware is evaluated. Performance evaluated for power quality of three-level diode clamped SPWM Voltage source inverter. FFT (Fast Fourier Transform) graph for DC-TLI and line current THD (Total Harmonic Distortion) values is compared with two-level inverter line voltage and current. MLIs (multilevel inverters) are utilised to increase the number of steps to produce high quality output waveforms. MLIs are used to eliminate harmonics and increase the inverter's performance.

Keywords: Power Quality, Solar PV Grid, Diode Clamped Three-Level Inverter, Photovoltaic, Grid-connected, renewable energy.

1 Introduction

The grid power quality is affected by the rising penetration of gridconnected renewable energy sources. Major power quality challenges include harmonics, frequency variation, and voltage fluctuation. Multilevel inverters are extensively employed in grid-tied PV systems because of their characterized by lower cost and higher efficiency. Owing to the extensive use of nonlinear power electronics loads, ac distribution networks have suffered significant harmonic pollution. Nonlinear loads like lamp ballasts, motors drives, electric welding equipment, arc furnaces, electronics battery chargers, etc. Harmonic standards and guidelines, such as IEEE-519-1992 and IEC 61000, govern best practices in power system and nonlinear equipment design[1].

Many strategies can be used to improve the power quality of inverters. This research develops a system that incorporates a three-level neutral point clamped (3L-NPC) inverter with a control strategy that keeps the necessary voltages for the input DC bus voltage of a grid-tied three-phase PV system [3]. The multilevel inverter (MLI) for solar inverter systems improves through increased rating and improving performance and efficiency. The rating of MLI is increased by adding more voltage levels without increasing individual device ratings, and the output voltage's harmonics are decreased. The three topologies of MLIs are: (1) Cascade H-bridge Multilevel Inverter (CHBMLI), (2) Flying Capacitor Multilevel Inverter (FCMLI), and (3) Diode Clamped Multilevel Inverter (DCMLI) [2]. For power quality enhancement, the researchers have consistently used, modified, tested, and implemented various MLI configurations for a wide range of applications for medium/high power and medium/high voltage systems[3][4].

Harmonics must be restricted to a specific level, according to the IEEE standard; otherwise, the core of power transformer may be saturated. Harmonics might be restricted in this scenario in two ways: on the load side or the source side. A power conditioner is commonly connected across the load at the point of common coupling (PCC). Precision inverter and controller design gives control over harmonics at source side [5][6].

A general SVPWM algorithm is proposed for three-level inverter [5][7]. Inverter control and output voltage with losses are described[8]. Solar fed multilevel inverter power quality improvement is discussed [9]. Reactive

power compensation and various control schemes of the inverter are addressed[10].

This research provides a clarification to ease the DC-TLI reduce complexity and improve power quality in a solar power inverter circuit. The paper reviews importance of DC-TLI, various PWM techniques used in MLI. Finally, a comparison of results between traditional two-level inverter and DC-TLI for power quality enhancement. The FFT graph for the load current of the proposed DC-TLI based PV system is measured, analysed, and discussed.

2. Proposed system



Figure 1. Block diagram for solar PV grid integration

The proposed solar PV grid integration block diagram is exposed in Figure 1. The system blocks represent (1) Solar panel (2) MPPT DC to DC boost converter (3) NPC three-level three phase inverter (4) three phase harmonics filter (5) main utility grid. Among the three topologies of MLIs, DCMLI is introduced. The output power is integrated with grid after the harmonics filter is used. The DC to AC converter use to convert DC in to AC. The MPPT control strategy is applied to the boost converter. The DC link voltage is controlled using constant voltage control mode. After applying the DQ transformation to DC to AC converter, the decoupling control structure calculates the three phase voltage to generate correct ac without harmonics. The DC-TLI output is synchronised with the main grid using phase locked loop (PLL) [3]. It transfers the required amount of power to the grid as per the load requisite. The switching operation of the inverter is determined by the SPWM control [11].

The DC-TLI have no dynamic voltage sharing problem, lower THD and low dv/dt compare to two level inverter. For more than three level, as level

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increases the number of clamping diodes also increases. The DC-TLI is widely utilised in high power medium voltage drive.

3. Simulation results

This paper presents a modelling and simulation work of grid connected three-level diode clamped SPWM inverter. MPPT controller used in PV grid system to get optimum output. The DC link voltage is connected with the DC-TLI and the output of the inverter is synchronized with the main grid. The inverter maintains the voltage and frequency equal to the grid voltage and frequency [11][12]. SIMULINK block sets in MATLAB are used for the simulation study.

The effectiveness of the suggested topology and control algorithm is tested and presented using simulation results. The simulation is done for the input value of solar irradiance is 1000 KW/m². SPWM scheme for implementation of twelve pulse generation for three-level diode clamped inverter is proposed as in Figure 3. Simulation parameters are shown in Table 1 used for DC-TLI. Figure 4 exhibits the results of SPWM gate pulse generation for DC-TLI.

Sr. No.	Parameter used in simulation	Values
1	Carrier Frequency	8000 Hz
2	Modulation Index	0.8
3	Output Voltage Frequency	50 Hz
4	Sample Time	50 e -6 S

Table 1. Inverter simulation parameters	Table	1. Inverter	simulation	parameters
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Figure 2. One leg configuration of SPWM DC-TLI

The frequency modulating index (M_f) and amplitude modulation index (M_a) are two important parameters to decide control of SPWM.

$$M_a = V_m / V_c \tag{1}$$

Where, $V_{m}=\mbox{amplitude}$ of modulating wave, $V_{c}=\mbox{amplitude}$ of carrier wave

$$\mathbf{M}_{\mathrm{f}} = \mathbf{f}_{\mathrm{c}}/\mathbf{f}_{\mathrm{m}} \tag{2}$$

Where, f_c = frequency of carrier wave, f_m = frequency of modulating wave



Figure 3. SPWM Scheme implementation for twelve pulse generation for DC-TLI



Figure 4. Gate pulses for one leg of SPWM DC-TLI

The DC-TLI output line voltages are shown in Figure 5 and phase voltages are shown in Figure 6. The output line current of each phase of the inverter is shown in Figure 7.



Figure 5. Line voltages of SPWM DC-TLI



Figure 6. Phase voltages of SPWM DC-TLI



Figure 7. Line currents of SPWM DC-TLI for different loading condition

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Figure 8. FFT graph for DC-TLI line current (rms)= 6.55 A and THD value = 2.76%

FFT Graph For DC-TLI line current (rms) of 6.55 A is shown in Figure 8. FFT Graph For two-level inverter Line current (rms) = 7A is shown in Figure 9.



Figure 9. FFT graph for two-level inverter line current (rms) = 7A and THD Value = 10.87%

Inverter type	Line current (rms)	THD
Two-level Three phase SPWM inverter for RL Load	7A	10.87%
DC-TLI SPWM inverter for RL Load	6.55A	2.76%

	Table 2. C	Comparison	of power	quality in	line current	on form	of THD
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4. Hardware results on DC-TLI SPWM Inverter (prototype)

The practical set up as shown in Figure 9 used to validate the solar powered DC-TLI for grid connection. The rating as simulation results with DC-TLI is presented in hardware also. Power rating is scaled to the following rating due to hardware availability.

- Inverter Input DC voltage 48V
- Maximum inverter output AC phase voltage (V_{ph}): 20 V
- Maximum inverter output AC line voltage (V_{L-L}): 34 V

Figure 10 shows the gate pulse of S_1 and S_1 ' and Figure 11 shows the gate pulse of S_1 and S_4 '. The waveform of line voltage (V_{RY}) is presented in Figure 12. Figure 13 shows FFT Graph for the line voltage waveform. Figure 14 shows for the three-level NPC inverter module phase voltage waveform.



Figure 10. Gate pulse of S1 and S1' for DC-TLI



Figure 11. Gate pulse of S1 and S4' for DC-TLI



Figure 12. Waveform of line voltage V_{RY} for DC-TLI



Figure 13. FFT Graph and line voltage waveform for DC-TLI



Figure 14. The waveform of phase voltages for DC-TLI

The Resistive (R) Load and Inductive (RL) Load connected with DC-TLI are experimentally checked. Resistive (R) Load of 200 ohm, 25 W is connected and experimentally checked as shown in Figure 15. Inductive (RL) Load of (R= 200 ohm, 25W, L=120mH each phase) is connected and experimentally checked as shown in Figure 16. The THD of line current is improved seen in practical testing.



Figure 15. Load Current in case of Resistive Load (R= 200 Ohm, 25 W) and FFT graph for DC-TLI

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Figure 16. DC-TLI waveform of Voltage (V_{RY}) and current (I_R) with RL Load (I_L =0.3A, V_L =34V)



Figure 17.Waveform of RL Load Current and FFT window graph for DC-TLI.

5. Conclusion

This paper presented a comparison between traditional two-level inverter and DC-TLI for power quality of solar PV systems. Power quality with respect to THD and Harmonic distortion is analysed for DC-TLI module for the solar PV grid. Simulation results of Three-level diode clamped

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SPWM VSI simulation using MATLAB are presented. FFT graph and THD values are compared for DC-TLI with two-level inverter line current. The 3-level diode clamped inverter improves THD up to 2.72% to 2-level conventional inverter THD is about 10.87 %. DC-TLI requires only six diode for clamping. As voltage level increases, clamping diode requirement also increases. Three-level inverters (TLIs) are used to eliminate harmonics and hence the performance of inverter system of the solar PV grid is improved.

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